## NOTICE OF APPEAL FROM THE PRIMARY EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

#16 Notice of Apper

ol Appeal |b|25|83

## PATENT APPLICATION

Inventor(S)

Serial No.

Yih-Feng Chyan

Case:

15-6-9

Group Art Unit: 2826

Filing Date

August 25, 2000

09/648164

Examiner.

Dickey

Printed name of person mailing paper ox fee)

I hereby certify that this Aurit (a of Possex is being deposited with the United States Postal Service "First Class Mail" on the

(Signature of person mailing paper or fee)

date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit 6-19-03

Title

Architecture For Circuit Connection Of A Vertical Transistor

## ASSISTANT COMMISSIONER FOR PATENTS WASHINGTON, D. C. 20231

SIR:

Applicant(s) hereby appeal(s) to the Board of Patent Appeals and Interferences from the decision dated March 19, 2003 of the Primary Examiner finally rejecting claims: 1, 13, and 14

The item(s) checked below are appropriate:

- [ ] A Petition for Extension of Time for reply to the rejections is attached.
- [X] Please charge the amount of \$330.00 covering the Appeal Fee (37 CFR 1.17(2)), to Agere Systems Deposit Account No. 501735. Duplicate copy of this letter is enclosed.
- [ ] Appeal Fee not required. (Fee was paid in prior Appeal.)

In the event of any non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 501735** as required to correct the error.

Please address all correspondence to Docket Administrator, Agere Systems Inc., 4 Connell Drive, Room 4U-533C, Berkeley Heights, NJ 07922-27474

Ferdinand M. Romano

Attorney for Applicant(s), Reg. No. 32752

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**TECHNOLOGY CENTER 2800** 

Date: June 19, 2003